REMARKS

Claims 1-18 are pending in the present application. The Examiner has indicated that claims 11-18 are allowed and that claims 2, 4, 5, 7, 9 and 10 would be allowable if rewritten to include all of the limitations of the claim(s) from which they depend.

Applicants respectfully request reconsideration of the application in view of the remarks appearing below.

Rejection Under 35 U.S.C. § 102

The Examiner has rejected claims 1 and 3 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,317,601 to Riordan et al., stating that Riordan et al. disclose an integrated circuit containing all of the limitations of these claims. Applicants respectfully disagree.

Riordan et al. disclose a clock distribution system for an integrated circuit device. The clock distribution system comprises a clock generator (12) that includes a counter (60), which is clocked by the falling edges of a PLL4x signal and generates signals at multiple frequencies, i.e., 2x, 1x, x/2, x/4, x/8 and x/16. The 2x, 1x, x/2 and x/4 signals are provided to a set of 4:1 multiplexers (65) that allow for selection from among these four input signals. The output of one of the 4:1 multiplexers is provided to a latch 77 that causes a one-quarter cycle, i.e., 90°, phase delay so that a "4x+90°" signal has its transitions synchronized to the falling edges of PLL4x signal, whereas the transitions of the other signals output by multiplexers (80), i.e., signals PLL1x, 4x, 2x and 1x, are synchronized to the rising edges of PLL4x signal.

Regarding claims 1 and 3, each of these claims, requires among other things, a phase detector operatively configured to detect an offset between a first phase of a selected one of a plurality of first signals and a second phase of a second signal and generate a third signal representing the offset. Relative to the phase detector limitation, in the Office Action the Examiner asserts that latch 77 of the Riordan et al. clock distribution system is a phase detector. Applicants respectfully disagree.

Latch 77, as it is used in the context of the Riordan et al. clock distribution system, is not a phase detector, but rather simply a delay element that causes the 90° phase delay of the 4x+90° signal as discussed above. It is clear from the language of independent claim 1 and the rest of the present application that the phase detector is an element that detects a variable offset between first and second signals and outputs a third signal that represents, i.e., indicates, the magnitude of

the offset. The offset information is subsequently used to control an aspect of the system of the present invention in a manner that is dependent upon the magnitude of the offset.

In contrast, in the Riordan et al. latch 77, there is no variability in the offset between the two input signals and, therefore, there is no variable offset to be detected. There is also no aspect of the Riordan et al. system that needs to be controlled as a function of a variable offset. Applicants assert that given the function of latch 77 in the Riordan et al. system, it is not reasonable to say that latch 77 generates a third signal representing the offset between first and second signals. The signal generated by latch 77 is merely a 90° phased-delayed signal. Consequently, latch 77 may be fairly characterized as a delay element, but not a phase detector.

Since Riordan et al. do not disclose at least the phase detector limitation of claims 1 and 3, the Riordan et al. patent cannot anticipate these claims. Therefore, Applicants respectfully request that the Examiner withdraw the present rejection.

Rejection Under 35 U.S.C. § 103

The Examiner has rejected claims 6 and 8 under 35 U.S.C. § 103 as being obvious in view of the Riordan et al. patent, discussed above, and further in view of ordinary skill in the art, stating that Riordan et al disclose a system containing all of the limitations of these claims except a plurality of microprocessors. The Examiner then states that systems containing a plurality of microprocessors are well known and asserts that it would have been obvious to a person having ordinary skill in the art at the time of the invention to implement the Riordan et al. system in the context of a multiprocessor system. Applicants respectfully disagree.

First, claims 6 and 8 each require, among other things, a phase detector that generates a third signal representing a phase offset between first and second signals. As discussed above in connection with the anticipation rejection, Riordan et al. do not disclose such a phase detector. Nor would it be obvious to someone skilled in the art to provide the Riordan et al. clock distribution system with a phase detector as claimed for the simple reason that the Riordan et al. system does not require such a phase detector. Consequently, any combination of the Riordan et al. patent and ordinary skill in the art would lack the phase detector of claims 6 and 8.

Second, claims 6 and 8 each also require a synchronization initiation circuit in electrical communication with a phase detector of each of a plurality of processors and operatively configured to provide a synchronization signal to each of the phase detectors for initiating detection of the phase offsets. Riordan et al. are completely silent on such a synchronization

initiation circuit. Furthermore, even if multiple processors were each provided with a Riordan et al. latch 77 in accordance with the Examiner's assertion, it would not be obvious to someone having ordinary skill in the art to provide a synchronization circuit to trigger these latches to detect an offset. This is so because, as described above, latch 77 is a delay element that does not require triggering for the purpose of synchronization.

Since any combination of the Riordan et al. patent and ordinary skill in the art would lack at least the phase detector and synchronization initiations circuit of claims 6 and 8, the cited combination cannot render these claims obvious. Therefore, Applicants respectfully request that the Examiner withdraw the present rejection.

CONCLUSION

In view of the foregoing, Applicants submit that claims 1-18 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

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